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09/755,164	01/08/2001	Nestor A. Bojarczuk, JR.	YOR9-2000-0642	4431

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/755,164	Applicant(s) BOJARCZUK, ET AL.	
	Examiner Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on th cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT E
TECHNOLOGY CENTER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 30, 2003 have been fully considered but they are not persuasive. The applicant points out that the Nishizawa, Ma, Yamazaki, and Goldman references do not disclose the advantages of an aluminum nitride layer. However the examiner does not believe this argument is pertinent since the above references disclose the claimed gate dielectric structure. Furthermore, it is understood that the silicon oxide layer in the Yamazaki reference is silicon dioxide.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al. (USPN 4,939,571).

4. In reference to claim 1, Nishizawa et al. (USPN 4,939,571, hereinafter referred to as the "Nishizawa" reference) discloses a similar device. Figure 1 of Nishizawa

discloses a field effect transistor having a substrate (5), a source (1), a drain (3) and a channel region (2). There is an insulating layer (6) disposed over the channel region (2). There is a gate electrode (4) which is disposed over the insulating layer (6). Nishizawa discloses that the composite insulating layer (6) contains aluminum nitride and aluminum oxide (column 2, lines 9-11).

5. With regard to claim 2, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." The examiner believes that this phrase covers every combination of the stated four dielectric layers. Thus it is the examiner's belief that this phrase meets the applicant's limitation where the aluminum nitride is "disposed over said aluminum oxide."

6. In reference to claim 3, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." It is the examiner's belief that this phrase meets the applicant's limitation where the aluminum nitride is "disposed under said aluminum oxide."

7. With regard to claim 4, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." It is the examiner's belief that this phrase meets the applicant's limitation where a layer of silicon dioxide is "disposed upon said channel region, said aluminum nitride disposed over said silicon dioxide."

8. In reference to claim 5, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." It is the examiner's belief that this phrase meets the applicant's limitation where a layer of silicon dioxide is "disposed over said channel region, said aluminum nitride disposed under said silicon dioxide."

9. In reference to claim 6, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." It is the examiner's belief that this phrase meets the applicant's limitation where a layer of silicon nitride is "disposed upon said channel region, said aluminum nitride disposed over said silicon nitride."

10. In reference to claim 7, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." It is the examiner's belief that this phrase meets the applicant's limitation where a layer of silicon nitride is "disposed over said channel region, said aluminum nitride disposed under said silicon nitride."

11. In reference to claim 14, Nishizawa discloses a similar device. Figure 1 of Nishizawa discloses a field effect transistor having a substrate (5), a source (1), a drain (3) and a channel region (2). There is an insulating layer (6) disposed over the channel region (2). There is a gate electrode (4) which is disposed over the insulating layer (6). Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." The examiner believes that this phrase covers every combination of the stated four dielectric

layers. Therefore it is the examiner's belief that this phrase meets the applicant's limitation where there is a "first layer comprising aluminum oxide disposed upon said channel region and a second layer comprising aluminum nitride is disposed upon said first layer."

12. In reference to claims 15 and 16, Nishizawa discloses a similar device. Figure 1 of Nishizawa discloses a field effect transistor having a substrate (5), a source (1), a drain (3) and a channel region (2). There is an insulating layer (6) disposed over the channel region (2). There is a gate electrode (4) which is disposed over the insulating layer (6). Nishizawa discloses that the insulating layer (6) contains aluminum nitride (column 2, lines 9-11). In addition, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." The examiner believes that this phrase covers every combination of the stated four dielectric layers.

13. In reference to claims 17 and 18, Nishizawa discloses such a multi-terminal device. Figure 1 of Nishizawa discloses a field effect transistor having a substrate (5), a source (1), a drain (3) and a channel region (2). There is an insulating layer (6) disposed over the channel region (2). There is a gate electrode (4) which is disposed over the insulating layer (6). Nishizawa discloses that the insulating layer (6) contains aluminum nitride (column 2, lines 9-11). In addition, Nishizawa discloses (in column 2, lines 9-11) that the insulating layer (6) is made with "SiO_2, Al_2O_3, Si_3N_4, or AlN, or their mixture, or their composite insulating layer." The examiner believes that this phrase covers every combination of the stated four dielectric layers.

14. Claims 1, 2, 6, and 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ma et al. (USPN 6,407,435 B1).

15. In reference to claims 1 and 2, Ma et al. (USPN 6,407,435 B1, hereinafter referred to as the "Ma" reference) discloses a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

16. In reference to claim 6, Ma that the first insulating layer (170) can be silicon nitride (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

17. In reference to claim 14, figure 4 of Ma describes a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

18. In reference to claims 15 and 16, Ma discloses a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

19. In reference to claims 17 and 18, Ma discloses such a multi-terminal device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

20. Claims 1, 4, and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki (USPN 5,094,966).

21. With regard to claims 1, 4, and 15-18, Yamazaki (USPN 5,094,966) discloses a similar device. Figure 1 of Yamazaki illustrates a multi-terminal device in the form of a field effect transistor which has a substrate (1), a source (6), a drain (7) and a channel region (not labeled). There is an insulating layer (5a, 5b) disposed over the channel

region. There is a gate electrode (4) which is disposed over the insulating layer (5a, 5b). Yamazaki discloses (column 4, lines 46-50) that the insulating layer (5a, 5b) is made of one layer of silicon dioxide (5a) and a layer of aluminum nitride (5b).

22. Claims 1-4, 7, and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Goldman et al. (USPN 4,151,537).

23. With regard to claims 1, 4, and 14-18, Goldman et al. (USPN 4,151,537, hereinafter referred to as the "Goldman" reference) discloses a similar device. Goldman illustrates a multi-terminal device in the form of a field effect transistor which has a substrate (12), a source (14), a drain (16) and a channel region (18). There is an insulating layer (22, 24, 26) disposed over the channel region (18). There is a gate electrode (28) which is disposed over the insulating layer (22, 24, 26). Goldman states (column 2, lines 61-65) that the top insulating layer (22) can be silicon nitride, the middle insulating layer (24) can be silicon oxynitride, and the bottom insulating layer (26) can be silicon dioxide. However, Goldman also discloses (column 2, lines 65-68) that any of the layers of the insulating layer (22, 24, 26) can be made of aluminum nitride or aluminum oxide; thereby meeting claims 1, 4, and 15-18.

24. In reference to claim 2, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where the aluminum nitride is "disposed over said aluminum oxide."

25. In reference to claim 3, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where the aluminum nitride is "disposed under said aluminum oxide."

26. With regard to claim 4, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where a layer of silicon dioxide is "disposed upon said channel region, said aluminum nitride disposed over said silicon dioxide."

27. In reference to claim 7, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where a layer of silicon nitride is "disposed over said channel region, said aluminum nitride disposed under said silicon nitride."

28. In reference to claim 14, Goldman discloses a similar device. Goldman illustrates a field effect transistor which has a substrate (12), a source (14), a drain (16) and a channel region (18). There is an insulating layer (22, 24, 26) disposed over the channel region (18). There is a gate electrode (28) which is disposed over the insulating layer (22, 24, 26). Goldman states (column 2, lines 61-65) that the top insulating layer (22) can be silicon nitride, the middle insulating layer (24) can be silicon oxynitride, and the bottom insulating layer (26) can be silicon dioxide. However, Goldman also discloses (column 2, lines 65-68) that any of the layers of the insulating layer (22, 24, 26) can be made of aluminum nitride or aluminum oxide. Therefore, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where there is a "first layer comprising aluminum oxide disposed upon said channel region and a second layer comprising aluminum nitride is disposed upon said first layer."

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
July 14, 2003